We Claim:

1. In a process integration scheme for forming a buried LOCOS collar in a trench vertical DRAM capacitor, the improvement that avoids widening of the trench at the height of the buried strap and avoidance of reduction of free trench diameter by placing the collar outside of the trench, comprising:

a) forming a DT etch in a substrate, depositing a first nitride layer on walls of the DT, filling the trench with a sacrificial poly silicon, planarizing and poly recessing to obtain a depth above a later formed STI isolation;

b) depositing a dielectric layer different from said first nitride layer in the trench;

c) opening the first nitride/dielectric layer/second nitride stack in said trench by a RIE, and recessing the sacrificial trench poly to a depth that corresponds to a desired lower end of the collar and that defines the depth at which the bottle and buried plate are formed in a later processing step;

d) etching to remove the nitride layer from silicon sidewalls in the recessed part of the trench and to remove the top nitride layer from the mask, and etching the silicon to:

I. create a recess large enough to place the collar oxide outside the trench; and

II. create a trench shape that allows uniform LOCOS oxidation;

e) affecting LOCOS oxidation that has an upper and

lower limit due to said first and second nitride layers, and forms bird's beaks between the dielectric layer different from said nitride layer and said second nitride layer, said LOCOS oxide thickness being chosen to suppress vertical transitor action;

f) depositing a second mask layer system of nitride/dielectric layer to provide a layer on top of the LOCOS oxide for gas phase doping and to protect said layer stack during sacrificial poly strip;

g) affecting RIE to open the nitride/dielectric stack and the LOCOS oxide at the trench poly and stripping the sacrificial poly while protecting trench sidewalls by the nitride layer;

h) stripping nitride from the trench sidewall and from the mask, affecting on oxide etch, and preparing a bottle formation and gasphase doping such that said bottle formation and gasphase doping are self aligned;

i) depositing a node dielectric layer;

j) affecting a trench poly fill and poly recessing to create a position of a LOCOS oxide; and

k) etching the node dielectric, affecting a nitride etch to expose the trench sidewalls, affecting a buried strap nitridation of the silicon walls, affecting a buried strap poly deposition, planarizing and recessing to an upper position of the buried strap, and forming a TTO.

2. The process of claim 1 wherein in step b), said dielectric layer different from said nitride layers is an oxide layer that serves as a mask for later processing.

3. The process of claim 1 wherein in step b), said dielectric layer different from said first nitride layer is created by radical assisted oxidation.

4. The process of claim 1 wherein said first and second nitride layers are deposited by LPCVD.

5. The process of claim 2 wherein, in step b), a second nitride layer is deposited on said dielectric layer; said second nitride layer serving to protect the oxide mask during sacrificial poly strip.

6. The process of claim 1 wherein, in step d), after the nitride etch the oxide mask is stripped.

7. The process of claim 5 wherein, in step e), said LOCOS oxide thickness that suppresses vertical parasitic transitor action is about 300A.

8. The process of claim 7 wherein said LOCOS oxidation is thermal oxidation at temperatures between about 1000°C and about 1,200°C to assure uniform oxide thickness.

9. The process of claim 1 wherein step f), said dielectric layer different from said nitride layers is an oxide layer.

10. The process of claim 9 wherein a RIE is used to open the nitride/oxide/nitride stack.

11. The process of claim 10 wherein said node is a node nitride.

12. A vertical DRAM capacitor prepared by the process of claim 1, and characterized by: a buried collar fabricated after DT etch and before trench processing; self aligned bottle and gas phase doping; no consumption of silicon at the depth of the buried strap; and no reduction of trench diameter.

13. A vertical DRAM capacitor formed by the process of claim 2.

14. A vertical DRAM capacitor formed by the process of claim 3.

15. A vertical DRAM capacitor formed by the process of claim 4.

16. A vertical DRAM capacitor formed by the process of claim 5.

17. A vertical DRAM capacitor formed by the process of claim 6.

18. A vertical DRAM capacitor formed by the process of claim 7.

19. A vertical DRAM capacitor formed by the process of claim 8.

20. A vertical DRAM capacitor formed by the process of claim 9.

21. A vertical DRAM capacitor formed by the process of claim 10.

22. A vertical DRAM capacitor formed by the process of claim 11.